11-08-05

Docket No. 8201/Y01/SYNX/JW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Re: Inventor(s): Michael R. Rice, Eric A. Englhardt, Vinay Shah, Martin R. Elliott, Robert B. Lowrance and Jeffrey C. Hudgens
Title: SYSTEMS AND METHODS FOR TRANSFERRING SMALL LOT SIZE SUBSTRATE CARRIERS BETWEEN PROCESSING TOOLS
Serial No.: 10/764,620
Filed: January 26, 2004
Examiner: Kasenge, Charles R
Group Art Unit: 2125

Transmitted herewith is:

X PTO Form 1449;

X Information Disclosure Statement, and sixty-seven cited references (copy of fifty-nine references enclosed); and

X Return Postcard.

FEE CALCULATION					
Fee Items	Claims Filed	Included With Basic Fee	Extra Claims	Fee Rate	Total
Total Claims	N/A	- 20 =	-0-	X $50.00	$0.00
Independent Claims	N/A	- 3 =	-0-	X $200.00	$0.00
Basic Filing Fee				$790.00	$0.00
TOTAL FEES					PAID

___ The Commissioner is hereby authorized to charge $0.00 to Deposit Account No. 04-1696.

XX The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **04-1696**. A duplicate copy of this transmittal is enclosed.

XX Please address all future correspondence to:

Customer # 41161
Dugan & Dugan, PC
55 South Broadway
Tarrytown, NY 10591

I hereby certify that this correspondence is being deposited with the United States Postal Service as express mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Express Mail Receipt No. EV605115695US

Date of Deposit: November 7, 2005

Signature: _____

Respectfully submitted,

_____

Brian M. Dugan
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Express Mail Label No. EV605115695US

PATENTS
8201/Y01/SYNX/JW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	:	Michael R. Rice, Eric A. Englhardt, Vinay Shah, Martin R. Elliott, Robert B. Lowrance and Jeffrey C. Hudgens
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INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97, applicants wish to call the attention of the Examiner to the following references:

U.S. Patent No. 5,544,350, Hung et al.

U.S. Patent No. 5,612,886, Yi-Cherng Weng

U.S. Patent No. 5,818,716, Chin et al.

U.S. Patent No. 5,825,650, Tza-Huei Wang

U.S. Patent No. 5,971,585, Dangat et al.

U.S. Patent No. 6,128,588, Guillermo Rudolfo Chacon

U.S. Patent No. 6,196,001, Tannous et al.

U.S. Patent No. 6,415,260, Yang et al.

Foreign Art Reference No. JP 55091839 A (Japan)

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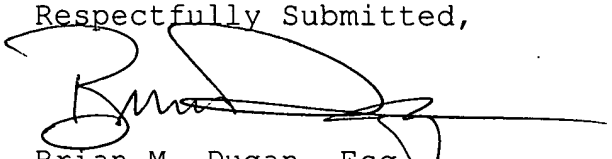
Nagesh, Sukhi et al., "Intelligent second-generation MES solutions for 300mm fabs", 2000, Solid State Technology, Vol. 43 No. 6, Pgs. 133-134, 136, 138.

These references are also listed on the accompanying Information Disclosure Statement (Form PTO-1449).

Consideration of the foregoing in relation to this patent application is respectfully requested.

Respectfully Submitted,



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Dated: November 7, 2005
Tarrytown, New York

U.S. Department of Commerce, Patent and Trademark Office	Docket No.: 8201/Y01/SYNX/JW	Serial No.: 10/764,620
LIST OF RELEVANT ART CITED BY APPLICANT (Use several sheets if necessary)	Applicants: Michael R. Rice, et al	
	Filing Date: January 26, 2004	Group: 2125

U.S. Patent Documents

*Examiner Initial		Document Number	Issue Date	Name	Class	Subclass	Filing Date If Appropriate
	US-1	5,544,350	08/06/96	Hung et al.			
	US-2	5,612,886	03/18/97	Yi-Cherng Weng			
	US-3	5,818,716	10/06/98	Chin et al.			
	US-4	5,825,650	10/20/98	Tza-Huei Wang			
	US-5	5,971,585	10/26/99	Dangat et al.			
	US-6	6,128,588	10/03/00	Guillermo Rudolfo Chacon			
	US-7	6,196,001	03/06/01	Tannous et al.			
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	F-3	JP 60049623 A	03/18/85	Japan			Abstract	
	F-4	JP 01181156 A	07/19/89	Japan			Abstract	
	F-5	JP 01257549 A	10/13/89	Japan			Abstract	

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	OT-3	Prasad, K., "A generic computer simulation model to characterize photolithography manufacturing area in an IC FAB facility", Sept. 1991, IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. 14 No. 3, Pg. 483-7.

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	F-8	JP 05290053 A	11/05/93	Japan			Abstract	
	F-9	JP 06260545 A	09/16/94	Japan			Abstract	
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	OT-4	Ehteshami, B. et al., "Trade-offs in cycle time management: hot lots", May 1992, IEEE Transactions on Semiconductor Manufacturing, Vol. 5 No. 2, Pg. 101-6.
	OT-5	Lou, S. et al., "Using simulation to test the robustness of various existing production control policies", 1991, 1991 Winter Simulation Conference Proceedings, IEEE, Pg. 261-9.
	OT-6	Berg, R. et al., " The formula: world class manufacturing for hybrid thin-film component production", 1992, IEEE/SEMI International Semiconductor Manufacturing Science Symposium, Pgs. 53-60.

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	F-13	JP 11176717 A	07/02/99	Japan			Abstract	
	F-14	JP 11296208 A	10/29/99	Japan			Abstract	
	F-15	JP 01332464 A	11/30/01	Japan			Abstract	

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	OT-7	Naguib, H., "The implementation of total quality management in a semiconductor manufacturing operation", 1992, IEEE/SEMI International Semiconductor Manufacturing Science Symposium, Pg. 63-7.
	OT-8	Rose, D., " Productivity enhancement", 1992, IEEE/SEMI International Semiconductor Manufacturing Science Symposium, Pg. 68.
	OT-9	Narayanan, S. et al., "Object-oriented simulation to support operator decision making in semiconductor manufacturing", 1992, 1992 IEEE International Conference on Systems, Man and Cybernetics, Vol. 2, Pg 1510-15.

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	F-16	JP 03007584 A	01/10/03	Japan			Abstract	
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	OT-20	Padillo, J. M. et al., "A strategic domain: IE in the semiconductor industry", March 1998, IIE Solutions, Pgs. 36-40, 42.
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	US-87						
	US-88						

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	F-37							
	F-38							
	F-39							
	F-40							

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	OT-23	Iriuchijima, K. et al., "WIP allocation planning for semiconductor factories", 1998, Proceedings of the 37th IEEE Conference on Decision and Control, Vol. 3, Pg. 2716-21.
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U.S. Department of Commerce, Patent and Trademark Office LIST OF RELEVANT ART CITED BY APPLICANT (Use several sheets if necessary)	Docket No.: 8201/Y01/SYNX/JW	Serial No.: 10/764,620
	Applicants: Michael R. Rice, et al	
	Filing Date: January 26, 2004	Group: 2125

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*Examiner Initial		Document Number	Issue Date	Name	Class	Subclass	Filing Date If Appropriate
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